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Perimeter leakage current in polymer light emitting diodes

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Abstract

Observation of leakage current paths through the device perimeter in standard poly(phenylene vinylene)-based light-emitting devices is reported. Perimeter leakage currents govern the diode performance in reverse and low positive bias and exhibit an ohmic character. Current density correlates with the perimeter-to-area ratio thus indicating that leakage currents are mainly confined on polymer regions in the vicinity of metallic contact limits (device perimeter).

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Keywords: Leakage currents; Edge shunt; Light emitting diodes

1. Introduction

Organic light-emitting diodes (OLEDs) have attracted much attention because of their potential applications in flat panel and flexible displays, data communication, and lighting systems. Among other technological requirements, taking control over diode leakage currents is one of the determining aspects of the device performance. From a portable system designer's point of view, leakage current may have dramatic negative effect on the standby life of the battery-powered device. Therefore, the physical origin of leakage currents in OLEDs should deserve much attention for reliable device engineering. There are some indications which relate the surface roughness of indium tin oxide substrates to the device leakage paths [1]. It is also believed that local damage of the organic layer induced during radio frequency or dc cathode sputtering lies behind the conducting paths [2], and modifications of the deposition techniques have been proposed to avoid such problem [3].

The measured current–voltage (J–V) characteristics in polymer and small-molecule light-emitting devices (OLED) in reverse and forward bias direction up to approximately the built-in potential V_{BI} often exhibits ohmic response. This behavior is believed to be caused by additional leakage currents flowing in parallel with useful currents responsible for the device operation, $J_{tot} = J_{oper} + J_{leakage}$. For voltages more positive than V_{BI} a current increase starts indicating the potential-driven enhancement in charge carrier injection. The existence of leakage currents governing the diode performance in reverse and low positive bias is well-known in inorganic electronics [4]. These effects are usually assimilated into a "shunt resistance" which accounts for the deviations from the ideal diode response. Such shunt resistance might be originated either by bulk processes or edge leakage paths. Apart from the importance of regarding leakage currents in complete device modeling [5], practical applications of light-emitting diodes and other types of organic devices should take into account the influence leakage current might have on the overall system performance. For instance, operating currents involved in small-area devices (100–300 μm diameter), like

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those devised for data communication systems [6], could be masked by leakage currents within a wide voltage range. In other cases, a proper determination of V_{BI} relies on a subtraction of the leakage current contribution. In this work the origin of leakage currents in a set of polymer light-emitting devices is explored and described their scaling behavior with respect to device geometry.

2. Results and discussion

In good accordance the general pattern discussed above, typical J–V characteristics in Fig. 1 of standard poly(phenylene vinylene)-based (PPV) light-emitting devices (different active areas) show both the ohmic low-voltage response and the current increment at $V > V_{BI}$. As observed in Fig. 1, the current onset is shifted toward more positive bias as $J_{leakage}$ increases thus indicating that the current onset and V_{BI} cannot be straightforwardly identified. Importantly, Fig. 1 makes apparent that $J_{leakage}$ measured in the ohmic response voltage range simply do not scale with the device area. Instead J_{oper} do scale with it as expected. Therefore usual 1-D device models should be revised in order to account for the leakage current effect.

The experiments indicated that $J_{leakage}$ has an ohmic character. As it will be next seen, the leakage currents exhibit a good correlation with the device perimeter. This fact reveals the importance of regarding perimeter diode regions in the edge of the metallic contact, in contrast to inner zones, for the system modeling. In this study PPV co-polymer has been used, "super yellow" (SY) prepared by Merck OLED Materials GmbH, as the light-emitting polymer. Standard device layouts were prepared, using a 200 nm thick [poly(ethylenethioxythiophene):poly(styrene-sulfonic) acid, PEDOT:PSS] hole injection layer, and a 100 nm thick SY layer which was covered with a 10 nm thick layer of barium. The anode comprises indium tin oxide (ITO) layers covered by a molybdenum/aluminium/molybdenum (MAM) layer at the positions where no light is to be generated. Such last layer is applied for contacting purposes and for decreasing the electrical resistance of the ITO electrode [7]. An additional 100 nm thick Al layer was evaporated on top of the cathode metal to protect the lower work function metals and serve as an optical mirror. Details on device preparation were published elsewhere [8]. J–V characteristics were collected using an AutoLab PGSTAT30 equipment (Fig. 1). Devices with three different active areas were tested: A (6.03 cm^2), B (0.11 cm^2) and C (0.01 cm^2).

By examining Fig. 1 one observes that the current density is independent of the device area for usual operating bias, but differs for $V < V_{BI}$. The simpler approach to dealing with this discrepancy may be to consider a difference in charge carrier injection between perimeter and center regions of the device. Provided the ohmic character of the device leakage currents, and assuming perimeter rather than area effects, one can write the total current density as

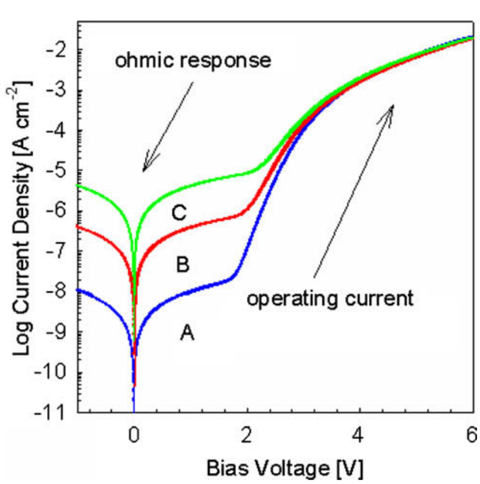

Fig. 1. J–V characteristics of OLEDs with structures ITO/PEDOT:PSS/SY/Ba with different device active areas: A (6.03 cm^2), B (0.11 cm^2) and C (0.01 cm^2).

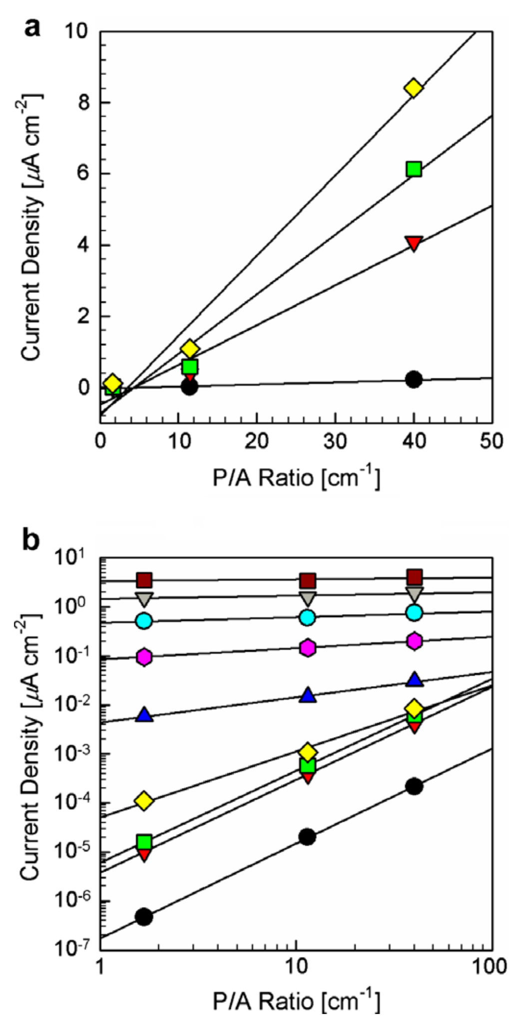

Fig. 2. J–P/A curves (same data in Fig. 1) as a function of the bias voltage: (a) 2.0, 1.5, 1.0, and 0.5 V from top to bottom in a linear scale (solid lines correspond to linear fits). (b) 4.5, 4.0, 3.5, 3.0, 2.5, 2.0, 1.5, 1.0, and 0.5 V from top to bottom in a log–log scale (solid lines correspond to power-law fits).

$$J_{\text{tot}} = J_{\text{oper}} + \frac{V}{R_0}\frac{P}{A} \tag{1}$$

where P stands for the device perimeter, A corresponds to the active area, and R_0 is a resistivity-related parameter with dimensions Ω cm. This equation states that J_{leakage} is proportional to the perimeter-to-area ratio at low-voltages, in which $J_{\text{tot}} \approx J_{\text{leakage}}$, whereas J_{tot} is independent of P/A in the bias range such that $J_{\text{tot}} \approx J_{\text{oper}}$. J–V characteristics shown in Fig. 1 are replotted as a function of P/A in linear and logarithmic scales for different bias voltages in Fig. 2. It is again evident that J_{leakage} does not scale with the device area. One can find in a quite good approximation a linear relationship between J_{tot} and P/A as observed in Fig. 2a at low bias ($V < 2.5$ V). Since J_{leakage} do not scale with device area, center zones seem not to be playing a determining role. By examining Fig. 2b it is evident that the influence of the leakage current on J_{tot} is even present at $V = 3.5$ V. For more positive bias we find a constant J_{tot} value as expected. The log–log plot of Fig. 2b allows to check the validity of Eq. (1). We observed that instead of a simple linear relationship at low-voltages $J_{\text{tot}} \propto P/A$, a power-law is encountered as $J_{\text{tot}} \propto (P/A)^{\alpha}$ with $1.3 < \alpha < 1.9$. It should be noted here that Eq. (1) is a phenomenological relation which may find a proper generalization providing a detailed physical model for the perimeter effect on leakage currents. What is evident in any case from the correlation shown in Fig. 2 is that leakage currents are mainly confined in the vicinity of metallic contact limits (device perimeter).

To distinguish between perimeter and bulk mechanisms is a common practice in the analysis of current–voltage characteristics of GaAs diodes [9] and silicon solar cells[10]. In such devices there is ample evidence for the different role played by perimeter in contrast to bulk recombination processes [11]. The distinction between bulk and edge shunts in solar cells has been addressed in order to reduce leakage effects on the device efficiency [10]. Usually edge shunts (perimeter leakage) have great detrimental consequences and appear as a consequence of defects and impurities induced during device production. The suppression of local shunts entails passivation of edge defects by means of several techniques, like plasma or chemical etching.

In the specific case of OLEDs, as the device area is enlarged central regions play a more significant role with respect to the perimeter ones, then reducing the leakage current density. Provided the special layer patterning used during fabrication of these devices in which MAM layers cover ITO electrodes on non-emitting regions, it is tentatively proposed that perimeter leakage currents are originated by short paths created between MAM layers and the cathode metal in the limit of the optically active zones.

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